AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

1. (Currently amended) A boosting circuit, comprising:

a first charge pump circuit which contains a first capacitive section charged to a first voltage;

a second charge pump circuit which contains a second capacitive section charged to said first voltage;

a third charge pump circuit which contains a third capacitive section charged to said first voltage; and

a switching unit which connects said first charge pump circuit, [[and]] said second charge pump circuit and a first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from [[a]] said first node to a first internal circuit of a semiconductor device, and connects said first charge pump circuit, said second charge pump circuit, [[and]] said third charge pump circuit and a second node in series in response to a second switch signal and said control signal, such that a third voltage is outputted from [[a]] said second node to a second internal circuit of said semiconductor device.

2. (Currently amended) [[The]] A boosting circuit ~~according to claim 1~~, comprising:

a first charge pump circuit which contains a first capacitive section charged to a first voltage;

a second charge pump circuit which contains a second capacitive section charged to said first voltage;

a third charge pump circuit which contains a third capacitive section charged to said first voltage; and

a switching unit which connects said first charge pump circuit, said second charge pump circuit and a first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from said first node to a first internal circuit of a semiconductor device, and connects said first charge pump circuit, said second charge pump circuit, said third charge pump circuit and a second node in series in response to a second switch signal and said control signal, such that a third voltage is outputted from said second node to a second internal circuit of said semiconductor device,

wherein said switching unit comprises:

a first switching section which connects said first charge pump circuit and said second charge pump circuit in response to said control signal;

a second switching section which connects said second charge pump circuit and said first node in response to said control signal and said first switch signal;

a third switching section which connects said second charge pump circuit and said third charge pump circuit in response to said control signal and said second switch signal; and

a fourth switching section which connects said third charge pump circuit and said second node.

3. (Original) The boosting circuit according to claim 2, wherein a power supply generates said first voltage,

said first charge pump circuit comprises:

said first capacitive section whose first and second side electrodes are connected to said first switching section; and

a first backward direction current blocking element whose output is connected to said second side electrode of said first capacitive section and whose input is connected to said power supply, such that a backward current from said first capacitive section to said power supply is blocked,

said second charge pump circuit comprises:

said second capacitive section whose first side electrode is connected to said first switching section and whose second side electrode is connected to said second switching section and said third switching section; and

a second backward direction current blocking element whose output is connected to said second side electrode of said second capacitive section and whose input is connected to said power supply, such that a backward current from said second capacitive section to said power supply is blocked, and

said third charge pump circuit comprises:

said third capacitive section whose first side electrode is connected to said third switching section and whose second side electrode is connected to said fourth switching

section; and

a third backward direction current blocking element whose output is connected to said second side electrode of said third capacitive section and whose input is connected to said power supply, such that a backward current from said third capacitive section to said power supply is blocked.

4. (Original) The boosting circuit according to claim 3, wherein said first switching section comprises:

a first inverting element to which said control signal is inputted;

a second inverting element whose input is connected to an output of said first inverting element and whose output is connected to said first side electrode of said first capacitive section;

a first conductive type of a first transistor which is connected between said second side electrode of said first capacitive section and said first side electrode of said second capacitive section and which receives the output of said first inverting element; and

a second conductive type of a second transistor which is connected between said first side electrode of said second capacitive section and a ground potential and which receives the output of said first inverting element.

5. (Original) The boosting circuit according to claim 3, wherein said second switching section comprises:

a second switching section control circuit which outputs a second control signal in response to said control signal, said first switch signal and a voltage applied to said first node; and

said second conductive type of a third transistor which is connected between said first node and said second side electrode of said second capacitive section.

6. (Original) The boosting circuit according to claim 3, wherein said third switching section comprises:

a third switching section control circuit which outputs a third control signal based on said control signal, said second switching signal and a voltage of said second node; and

said second conductive type of a fourth transistor which connects said second side electrode of said second capacitive section and said first side electrode of said third capacitive section in response to said third control signal.

7. (Original) The boosting circuit according to claim 3, wherein said fourth switching section comprises:

a fourth switching section control circuit which outputs a fourth control signal based on said control signal, said second switching signal and a voltage of said second node; and

said second conductive type of a fifth transistor which connects said second side electrode of said third capacitive section and said second node in response to said fourth control signal.

8. (Original) The boosting circuit according to claim 3, wherein said switching unit further comprises a fifth switching section which comprises:

a fifth switching section control circuit which outputs a fifth control signal based on said control signal and said second switching signal; and

said second conductive type of a sixth transistor which connects said first side electrode of said third capacitive section and said ground potential in response to said fifth control signal.

9. (Original) The boosting circuit according to claim 5, wherein said first conductive type is a P-type and said second conductive type is an N-type, said second switcher control circuit comprises:

a first NAND circuit to which said first control signal and said first switch signal are inputted;

a third inverting device whose input is connected to an output of said first NAND circuit;

said second conductive type of a seventh transistor whose gate is connected to an output of said third inverting device and whose source is grounded;

a fourth inverting device whose input is connected to the output of said third inverting device;

said second conductive type of an eighth transistor whose gate is connected to an output of said fourth inverting device and whose source is grounded;

said first conductive type of a ninth transistor whose source is connected to said first node, whose gate is connected to a drain of said eighth transistor and whose drain is connected to a drain of said seventh transistor;

said first conductive type of a tenth transistor whose source is connected to said first node, whose gate is connected to the drain of said seventh transistor and whose drain is connected to the drain of said eighth transistor;

a fourth capacitive section whose negative electrode side is connected to the drain of said eighth transistor and whose positive electrode side is connected to the gate of said third transistor; and

a fourth back flow protecting device whose output is connected to the positive

electrode side of said fourth capacitive section and whose input is connected to said power source, for protecting a back flow to said power source from said fourth capacitive section.

10. (Original) The boosting circuit according to claim 6, wherein said first conductive type is the P-type and said second conductive type is the N-type, said third switcher control circuit comprises:

a second NAND circuit to which said first control signal and said second switch signal are inputted;

a fifth inverting device whose input is connected to an output of said second NAND circuit;

said second conductive type of an eleventh transistor whose gate is connected to an output of said fifth inverting device and whose source is grounded;

a sixth inverting device whose input is connected to the output of said fifth inverting device;

said second conductive type of a twelfth transistor whose gate is connected to an output of said sixth inverting device, whose drain is connected to the gate of said fourth transistor and whose source is grounded;

said first conductive type of a thirteenth transistor whose source is connected to said second node, whose gate is connected to a drain of said twelfth transistor and whose drain is connected to a drain of said eleventh transistor; and

said first conductive type of a fourteenth transistor whose source is connected to said second node, whose gate is connected to the drain of said eleventh transistor and whose drain is connected to the drain of said twelfth transistor.

11. (Original) The boosting circuit according to claim 7, wherein said first conductive type is a P-type and said second conductive type is an N-type, said fourth switcher control circuit comprises:

a third NAND circuit to which said first control signal and said second switch signal are inputted;

a seventh inverting device whose input is connected to an output of said third NAND circuit;

said second conductive type of a fifteenth transistor whose gate is connected to an output of said seventh inverting device and whose source is grounded;

an eighth inverting device whose input is connected to the output of said seventh inverting device;

said second conductive type of a sixteenth transistor whose gate is connected to an output of said eighth inverting device and whose source is grounded;

said first conductive type of a seventeenth transistor whose source is connected to said second node, whose gate is connected to a drain of said sixteenth transistor and whose drain is connected to a drain of said fifteenth transistor;

said first conductive type of an eighteenth transistor whose source is connected to said second node, whose gate is connected to the drain of said fifteenth transistor and whose drain is connected to the drain of said sixteenth transistor;

a fifth capacitive section whose negative electrode side is connected to the drain of said sixteenth transistor and whose positive electrode side is connected to the gate of said third transistor; and

a fifth back flow protecting device whose output is connected to the positive

electrode side of said fifth capacitive section and whose input is connected to said power source, for protecting a back flow to said power source from said fifth capacitive section.

12. (Original) The boosting circuit according to claim 8, wherein said second conductive type is an N-type,

said fifth switcher control circuit has a fourth NAND circuit to which said first control signal and said second switch signal are inputted and whose output is connected to the gate of said sixth transistor.

13. (Currently amended) A boosting circuit, comprising:

N ~~(N is an integer of two or more)~~ charge pump circuits to which a power supply voltage is applied, wherein N is an integer of two or more; and

a switching unit which connects [[the]] a first group of J ~~(J is an integer satisfying 2≤J≤N)~~ charge pump circuits among said N charge pump circuits and a first node in series in response to a control signal and a first switching signal, wherein J is an integer satisfying $2 \leq J \leq N$, to output a voltage equal to [[(]]J+1[[)]] times said power supply voltage from said first node to a first internal circuit of a semiconductor device, and which connects [[the]] a second group of K [[k]] ~~(k is an integer satisfying 2≤K≤N)~~ charge pump circuits among said N charge pump circuits and a second node in series in response to said control signal and a second switching signal, wherein K is an integer satisfying $2 \leq K \leq N$, to output a voltage equal to [[(]]K+1[[)]] times said power supply voltage from said second node to a second internal circuit of said semiconductor device.

14. (Currently amended) A semiconductor device, comprising:

a boosting circuit; and

first and second internal circuits connected to said boosting circuit via first and second nodes,

wherein said boosting circuit comprises:

a first charge pump circuit which contains a first capacitive section charged to a first voltage;

a second charge pump circuit which contains a first capacitive section charged to said first voltage;

a third charge pump circuit which contains a first capacitive section charged to said first voltage; and

a switching unit which connects said first charge pump circuit, [[and]] said second charge pump circuit and said first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from said first node to said first internal circuit, and connects said first charge pump circuit, said second charge pump circuit, [[and]] said third charge pump circuit and said second node in series in response to a second switch signal and said control signal, such that a third voltage is outputted from said second node to said second internal circuit.

15. (Currently amended) [[The]] A semiconductor device ~~according to claim 14~~, comprising:

a boosting circuit; and

first and second internal circuits connected to said boosting circuit via first and second nodes,

wherein said boosting circuit comprises:

a first charge pump circuit which contains a first capacitive section charged to a first voltage;

a second charge pump circuit which contains a first capacitive section charged to said first voltage;

a third charge pump circuit which contains a first capacitive section charged to said first voltage; and

a switching unit which connects said first charge pump circuit, said second charge pump circuit and said first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from said first node to said first internal circuit, and connects said first charge pump circuit, said second charge pump circuit, said third charge pump circuit and the second node in series in response to a second switch signal and said control signal, such that a third voltage is outputted from said second node to said second internal circuit,

wherein said switching unit comprises:

a first switching section which connects said first charge pump circuit and said second charge pump circuit in response to said control signal;

a second switching section which connects said second charge pump circuit and said first node in response to said control signal and said first switch signal;

a third switching section which connects said second charge pump circuit and said third charge pump circuit in response to said control signal and said second switch signal; and

a fourth switching section which connects said third charge pump circuit and said second node.

16. (Original) The semiconductor device according to claim 15, wherein a power supply generates said first voltage,

said first charge pump circuit comprises:

said first capacitive section whose first and second side electrodes are connected to said first switching section; and

a first backward direction current blocking element whose output is connected to said second side electrode of said first capacitive section and whose input is connected to said power supply, such that a backward current from said first capacitive section to said power supply is blocked,

said second charge pump circuit comprises:

said second capacitive section whose first side electrode is connected to said first switching section and whose second side electrode is connected to said second switching section and said third switching section; and

a second backward direction current blocking element whose output is connected to said second side electrode of said second capacitive section and whose input is connected to said power supply, such that a backward current from said second capacitive section to said power supply is blocked, and

said third charge pump circuit comprises:

said third capacitive section whose first side electrode is connected to said third switching section and whose second side electrode is connected to said fourth switching section; and

a third backward direction current blocking element whose output is connected to said second side electrode of said third capacitive section and whose input is connected to said power supply, such that a backward current from said third capacitive section to said power supply is blocked.

17. (Original) The semiconductor device according to claim 16, wherein said first switching section comprises:

a first inverting element to which said first control signal is inputted;

a second inverting element whose input is connected to an output of said first inverting element and whose output is connected to said first side electrode of said first capacitive section;

a first conductive type of a first transistor which is connected between said second side electrode of said first capacitive section and said first side electrode of said second capacitive section and which receives the output of said first inverting element; and

a second conductive type of a second transistor which is connected between said first side electrode of said second capacitive section and a ground potential and which receives the output of said first inverting element.

18. (Currently amended) A semiconductor device, comprising:

a boosting circuit; and

first and second internal circuits connected to said boosting circuit via first and second nodes,

wherein said boosting circuit comprises:

N ~~(N is an integer of two or more)~~ charge pump circuits to which a power supply voltage is applied, wherein N is an integer of two or more; and

a switching unit which connects [[the]] a first group of J ~~(J is an integer satisfying $2 \leq J \leq N$)~~ charge pump circuits among said N charge pump circuits and said first node in series in response to a control signal and a first switching signal, wherein J is an integer satisfying $2 \leq J \leq N$, to output a voltage equal to [[(]]J+1[[)]] times said power supply voltage from said first node to a first internal circuit of a semiconductor device, and which connects [[the]] a second group of K [[k]] ~~(k is an integer satisfying $2 \leq K \leq N$)~~ charge pump circuits among said N charge pump circuits and said second node in series in response to said control signal and a second switching signal, wherein K is an integer satisfying $2 \leq K \leq N$, to output a voltage equal to [[(]]K+1[[)]] times said power supply voltage from said second node to a second internal circuit of said semiconductor device.

19. (Currently amended) A method of boosting a voltage, comprising:

charging first and second capacitors to a first voltage in first and second modes;

boosting a potential of said first capacitor to twice that of said first voltage in said first and second modes;

connecting said first and second capacitors in series in said first mode to output a second voltage from a first node;

charging a third ~~capacitors~~ capacitor to said first voltage in said second mode;

[[and]]

connecting said first to third capacitor in series in said second mode to output a third voltage from a second node; and

switching between first and second modes in response to a control signal and first and second switch signals.

20. (Original) The method according to claim 19, further comprising:

supplying said second voltage to a first internal circuit of a semiconductor device; and

supplying said second voltage to a second internal circuit of said semiconductor device.